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PTO/SB/21 (01-03)
Approved for use through 9/30/00. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>		Application / Conf. No.	10/001,871 / 3401
Mail Stop:		Filing Date	November 19, 2001
Express Mail Receipt No.		First Named Inventor	Stephen M. Douglass
		Examiner Name	Unassigned
		Art Unit	2818 JAN 22 2004
		Patent No.	Technology Center 2100
Total Number of Pages in This Submission		Attorney Docket Number	X-919 US

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ENCLOSURES (check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Amendment / Reply <ul style="list-style-type: none"> <input type="checkbox"/> Preliminary Amendment <input type="checkbox"/> After Final <input type="checkbox"/> Affidavit(s)/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Change Status to LARGE ENTITY <input type="checkbox"/> Express Abandonment Request <input checked="" type="checkbox"/> Information Disclosure Statement (Supplemental) <input checked="" type="checkbox"/> Substitute PTO-1449(s) IDS by Applicant (PTO/SB/08A) <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/ Incomplete Application <ul style="list-style-type: none"> <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53 	<input type="checkbox"/> Assignment Papers (with Recordation Cover Sheet) <input type="checkbox"/> Declaration / Oath <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition - <input type="checkbox"/> To Convert a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund	<input type="checkbox"/> After Allowance Communication to <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Return Receipt Postcard <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): <div style="border: 1px solid black; padding: 5px; margin-top: 5px;"> One copy each of the One Hundred Two (102) References Cited </div>
Remarks		

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TC 2100

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

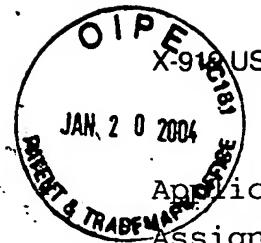
Firm or Customer Number	24309 (Customer Number)	Reg. Number 51,959
Attn:	Justin Liu	
Signature		
Date	January 16, 2004	Charge any additional fees required/credit any overpayment to our Deposit Account Number: 24-0040

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on this date: January 16, 2004

Typed or Printed Name	Julie Matthews	
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	Date	January 16, 2004

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.



PATENT

IN THE UNITED STATES PATENT OFFICE

Applicants: Stephen M. Douglass et al.
Assignee: Xilinx, Inc.
Title: "Method and Apparatus for Processing Data Within a
Programmable Gate Array Using Fixed and
Programmable Processors"

Serial No.: 10/001,871 File Date: November 19, 2001
Examiner: Unknown Art Unit: 2818
Docket No.: X-919 US Conf. No.: 3401

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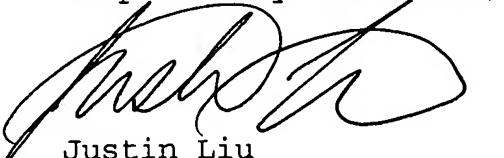
Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the One Hundred Two (102) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

These references were cited in related U.S. patent applications. This Information Disclosure Statement is being filed under 37 CFR 1.97(b) prior to the receipt of a first office action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,



Justin Liu
Attorney for Applicants
Reg. No. 51,959

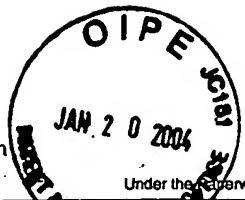
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Substitute Form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

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Complete if Known

Application / C nf. N .	10/001,871	/	3401
Filing Dat	November 19, 2001		
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Examiner Name	Unknown		
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U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No.'	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)	MM-DD-YYYY		
		US- 4,758,985	07-19-88	Carter	
		US- 5,142,625	08-25-92	Nakai	
		US- 4,855,669	08-08-89	Mahoney	
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¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Art Unit	2818		JAN 22 2004
Examiner Name	Unknown		

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OTHER - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		ANDRE' DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

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Date
Considered

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Application Number	10/001,871	/	3401
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First Named Inventor	Stephen M. Douglass		
Art Unit	2818		
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Attorney Docket Number	X-919 US		

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
	US- 5,473,267		12-05-95	Stansfield	
	US- 5,742,180		04-21-98	DeHon et al.	
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Applicant / Conf. No.	10/001,871	/	3401
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OTHER - NON PATENT LITERATURE DOCUMENTS

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Examiner Initials	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		CHRISTIAN ISELI et al., "AC++ COMPILER FOR FPGA CUSTOM EXECUTION UNITS SYNTHESIS," 1995, pp. 173-179, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		RALPH D. WITTIG et al., "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC, April 17, 1996, pp 126-135, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

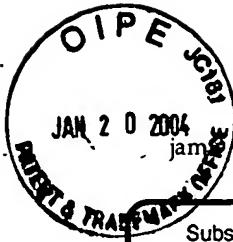
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		Number - Kind Code (if known)			
		US- 6,011,407	01-04-00	New	
		US- 6,172,990	01-09-01	Deb et al.	
		US- 6,510,548			
		US- 5,760,607	06-02-98	Leeds et al.	
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		US- 6,178,541	01-23-01	Joly et al.	
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